NetSpeed AHB converter LP spec

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About This Document

This document describes the NetSpeed AHB converter low power design implementation.

Audience

This document is intended for users of NocStudio:

* NoC Architects
* NoC Designers
* SoC Architects

Related Documents

The following documents can be used as a reference to this document.

* NetSpeed NocStudio User Manual

Related Documents

The following documents can be used as a reference to this document.

* NetSpeed NocStudio Orion User Manual
* NetSpeed Orion Physical Design Guidelines

Customer Support

For technical support about this product, please contact [support@netspeedsystems.com](mailto:support@netspeedsystems.com)

For general information about NetSpeed products refer to: [www.netspeedsystems.com](http://www.netspeedsystems.com)

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# Introduction

# ahb2axi lp Design Implementation

## constraints from ahblite protocol

Following are the AHB-lite protocol constraints on AHB2AXI converter. The LP solutions have to be designed around these constraints

* During reset, HREADY should be asserted high
* After coming out of reset, the HREADY should be asserted high to accept the Address phase of the request from the AHB master. Therafter ahb2axi can insert multiple wait states to backpressure through HREADY, but ultimately needs to complete the transaction.

1. When master asserts IDLE or BUSY, slave must respond with HREADY high, HRESP ok.

* For posted writes (HPROT[2] set to 1), all AHB-Lite write data beats receive an automatic OKAY response from the slave (ahb2axi in this case), irrespective of the B-channel AXI response.

## assumptions

* The ahb2axi converter must be in the same power domain as the AHB master.
* There is a single clock and reset at the interface of AHB master and ahb2axi, and the  
  state of those signals are consistent. The reset transitions are the same.
* The reset state for the power domains of ahb2axi and AXI master bridge should be considered to be in IDLE state, when they belong to different power domains. Even if they belong to the same power domain, the reset state of the power domain is considered to be IDLE
* Where ahb2axi is instantiated, the AHB host must not initiate new transactions when Q-channel is not in the Q-RUN state, i.e., no new transactions allowed when QREQn and QACCEPTn of the host PD are not both 1’b1

## LP V2 Protocol compliance

### Power up sequence

1. Coming out of reset, the AHB converter should be fencing for AXI master. It should be be idling it’s own interface driving sleep\_ack\_n and fence\_ack\_n low
2. NSPS drives sleep\_req\_n, reset\_pd\_n high to ahb2axi to allow transactions. Ahb2axi in turn drives sleep\_ack\_n high
3. NSPS asserts pd\_active\_<axi\_mstr\_PD> high to inform the ahb2axi should cease fencing/draining for its attached AXI master bridge.

### Ahb2axi Fence/Drain sequence for AXI master bridge

1. Upon 1->0 transition of pd\_active\_<axi\_mstr\_PD>, ahb2axi converter will look for next clean transaction boundary before fencing newly arriving transactions
2. Ahb2axi will have the option of two usual fencing behavior for newly arriving transactions
   1. Stall and autowake if the power domain of the attached AXI master bridge is wakeable
   2. Return ERROR on HRESP if the power domain of the attached AXI master bridge is NOT wakeable (Q3 target). The verification TB should be aware of the state of   
      pd\_active\_<axi\_mstr\_PD> and if it is AUTOWAKE enabled.
3. Ahb2axi needs to fence even when it has the same power domain as AXI master bridge. . Otherwise, AXI master could shut off its interface with pending transactions living in the converter. This is possible when the shared pd\_active\_<PD> is low, the AXI master bridge is in powered down mode and ahb2axi is not in powered down mode.
4. PMU honors the autowake signal, NSPS de-asserts sleep request and restores power to AXI master bridge.
5. After power is restored, the AXI master bridge asserts xxREADY signal high to accept new transactions from ahb2axi.
6. AHB converter will track completion of all transactions accepted prior to fencing boundary and will withhold fence\_ack\_n until all have completed.
7. Once all the outstanding transactions are complete, ahb2axi drives fence\_ack\_n low.
8. The NSPS then can initiate power down sequence for AXI master bridge by driving sleep\_req\_n low.

### Power down sequence of ahb2axi

1. NSPS asserts pd\_active\_<abh2axi\_PD> low to initiate power down sequence  
 2. NSPS will wait for fence\_ack\_n to be de-asserted if ahb2axi is already in the middle of  
 fence/drain. If there are no outstanding transactions for fence/drain, fence\_ack\_n will   
 already be in de-asserted state. Ahb2axi will drive fence\_done\_n high.  
 3. NSPS will initiate power down for ahb2axi by driving sleep\_req\_n low  
 4. Once ahb2axi is in true idle state, sleep\_ack\_n and fence\_done\_n will be driven low.

### LP I/O fence/drain signal list

|  |  |  |  |
| --- | --- | --- | --- |
| Signal Name | Direction | Purpose | Active/Clamp and Reset Values |
| pd\_active\_<axi\_mstr\_PD> | Input | Indicates whether the attached AXI master bridge is reachable via its power domain | 1/0 |
| pd\_active\_<ahb2axi\_PD> | Input | Indicates the pd\_active status of the power domain of ahb2axi | 1/0 |
| ahb2axi\_fence\_ack\_n | Output | Signal indicating fencing/draining associated with pd\_active\_<axi\_mstr\_PD> 1-> 0 transition has completed. Should remain asserted until 0->1 transition on pd\_active\_<axi\_mstr\_PD> | 0/0 |
| ahb2axi\_fence\_done\_n | Output | Inverted version of fence\_ack\_n, except when ahb2axi is going to sleep (i.e., it is asserting *sleep\_ack\_n*), it forces this signal low. | 0/0 |
| ahb2axi\_autowake\_axi | Output | Request to restore power in AXI master bridge in response to new transactions on ahb2axi interface | 1/0 |

### AUTOWAKE register

Ahb2axi will support an AUTOWAKE register and its reset value is determined by NocStudio parameter P\_MST\_AUTOWAKE\_ENB. NocStudio will use the same value for this parameter as the AXI master bridge that is driven by ahb2axi. The regbus address[12:0] of this register is 'h218 and is a R/W register, accessed via Regbus. Details are provided in “[AXI-ACE bridge Registers.xlsx](https://s3.amazonaws.com/uploads.hipchat.com/50167/2406457/OFzkRvjAweMNqMt/AXI-ACE%20bridge%20Registers.xlsx)” spreadsheet.

### NocStudio parameter requirement

1. P\_AXI\_BRIDGE\_PD\_AUTOWAKE\_ENB :This parameter when set to 1, indicates that the power domain of the AXI master bridge that the ahb2axi is driving is AUTOWAKE enabled.
2. P\_MST\_AUTOWAKE\_ENB : This is the reset value of AUTOWAKE register in ahb2axi. NocStudio will use the same value for this parameter as the AXI master bridge that is driven by ahb2axi. If set to 1, ahb2axi is capable of generating AUTOWAKE signal

### Enabling ahb2axi to AUTOWAKE the AXI master bridge

To enable ahb2axi to send AUTOWAKE signal to the power domain of the attached AXI master bridge, both the following conditions are required

* + Bit[0] of AUTOWAKE register in ahb2axi is set to 1
  + P\_AXI\_BRIDGE\_PD\_AUTOWAKE\_ENB parameter is set to 1

### Verification

Verification TB needs to be aware that if P\_AXI\_MST\_AUTOWAKE\_ENB = 0 and pd\_active\_<axi\_mstr\_PD> = 0, transactions from AHB host to ahb2axi will result in ERROR on HRESP. In such cases, the test should not FAIL for non delivery of the transaction to the intended target.

### Open Items from meeting:

Question : Does the ahb2axi converter support EARLY BURST TERMINATION from AHB host

And is the behavior different for LP cases ?

Answer : Yes, ahb2axi the converter currently supports EARLY BURST TERMINATION, and it’s behavior is not different for LP cases. It behaves the same for non LP and LP cases

Question : How should we be handling cases where successful completion for AHB POSTED WRITES fails after we have acknowledged back to the host with an OK response ?

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